

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of processing data comprising the step of: coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and the array comprising a configurable network;

wherein:

the at least one unit is operable independently of the array; and

the array is:

at least one of coarse grained and runtime reconfigurable; and
coupled ~~[[into]]~~ to the instruction pipeline.

2. (Currently Amended) A method according to claim 1, further comprising the step of:

transferring via at least one data path at least one of an input data and an output data ~~from between~~ the at least one unit to ~~[[and]]~~ the array and from the array to the at least one unit, the at least one data path being provided therebetween and comprising at least one FIFO so as to allow for at least one of (i) a coupling between the at least one unit and the array that is not strictly synchronous and (ii) a data processing within the at least one unit and the array that is not strictly synchronous.

3. (Previously Presented) A method according to claim 2, wherein the transferring is performed by at least one of inserting data directly into and extracting data directly from a data path of at least one of the at least one unit and the array.

4. (Previously Presented) A method according to claim 3, further comprising the step of:

providing between the at least one unit and the array a path adapted for transfer of at least one of status information and event information.

5. (Currently Amended) A device for processing data comprising:
at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and
an array adapted for processing data comprising a configurable network and a plurality of data processing cells that are configurable in their function;
wherein:

the array is coupled ~~[[into]]~~ to the instruction pipeline, the coupling of the array to the instruction pipeline including controlling configurations by the instruction pipeline; and

the at least one unit is operable independently of the array.

6. (Currently Amended) The device according to claim 5, wherein at least one of:
at least one data path is provided between the array and the at least one unit, the at least one data path comprising at least one FIFO that allows at least one of (i) a coupling between the at least one unit and the array that is not strictly synchronous and (ii) a data processing within the at least one unit and the array that is not strictly synchronous; and
data is transferred by at least one of extracting data directly from and inserting data directly into a data path of at least one of the at least one unit and the array.

7. (Currently Amended) A method of processing data comprising the steps of:
coupling:

(a) at least one unit adapted for processing data in a sequential manner and comprising an instruction pipeline; and

(b) an array adapted for processing data, the array comprising a plurality of data processing cells that are configurable in their function and the array comprising a configurable network; and

providing a path allowing for block data transfer from the array and at least one of a data cache and another data source.

8-11. (Canceled).

12. (Previously Presented) A method according to claim 1, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller.

13. (Previously Presented) A method according to claim 1, wherein the array includes at least one of a data processor, a Field Programmable Gate-Array (FPGA), a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaameleon-technology data processing fabric.

14. (Previously Presented) A method according to claim 2, wherein the at least one data path between the at least one unit and the array includes at least one local memory connected to the at least one unit as a cache and connected to the array.

15. (Previously Presented) A method according to claim 14, wherein the at least one local memory includes an internal RAM (IRAM).

16. (Previously Presented) A method according to claim 1, wherein configuration information for the array is issued by the instruction pipeline of the at least one unit.

17. (Previously Presented) A method according to claim 16, further comprising:
buffering the configuration information in at least one FIFO so as to allow for at least one of a coupling between and a data processing within the at least one unit and the array that is not strictly synchronous.

18. (Previously Presented) A method according to claim 1, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit.

19. (Previously Presented) A method according to claim 18, wherein the array is operable synchronously to the unit.

20. (Previously Presented) A method according to claim 4, wherein the at least one of the status information and the event information includes at least one of flags, an overflow, and a carry.

21. (Previously Presented) A device according to claim 5, wherein the at least one unit includes at least one of a CPU, a von-Neumann-Processor, and a microcontroller.

22. (Currently Amended) A device according to claim 5, wherein the array includes ~~at least one of~~ (a) a runtime ~~[[and]]~~ reconfigurable data processor, ~~(b) a Data Flow Processor (DFP), (c) a Digital Signal Processor (DSP), (d) an eXtreme Processing Platform (XPP), and (e) a chaameleon-technology data processing fabric.~~

23. (Previously Presented) A device according to claim 6, wherein the at least one data path includes at least one local memory connected to the unit as cache and connected to the array.

24. (Previously Presented) A method according to claim 23, wherein the at least one local memory includes an internal RAM (IRAM).

25. (Previously Presented) A device according to claim 5, wherein configuration information for the array is issued by the instruction pipeline.

26. (Currently Amended) A device according to claim 25, wherein the configuration information is buffered in at least one FIFO so as to allow for at least one of (i) a coupling between the at least one unit and the array that is not strictly synchronous and (ii) a data processing within the at least one unit and the array that is not strictly synchronous.

27. (Previously Presented) A device according to claim 5, wherein the at least one unit supports multi-threading, and the array is connected as a thread unit.

28. (Previously Presented) A device according to claim 27, wherein the array operates synchronously to the unit.

29. (Previously Presented) A method according to claim 7, wherein the at least one unit includes at least one of a CPU, a von-Neumann-processor, and a microcontroller.

30. (Previously Presented) A method according to claim 7, wherein the array includes at least one of a runtime and reconfigurable data processor, a Data Flow Processor (DFP), a Digital Signal Processor (DSP), an eXtreme Processing Platform (XPP), and a chaameleon-technology data processing fabric.